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PATENT
Client Docket No. TUC920030050US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Yu-Cheng Hsu et al.	
Serial No.:	10/686,878	
Filed:	October 16, 2003	Group Art Unit: 2136
For:	APPARATUS SYSTEM AND METHOD FOR DETERMINISTICALLY TRANSFERRING DATA BY REBOOTING TO A DATA TRANSFER KERNEL	
Examiner:	Carlton Johnson	

SUPPLEMENTAL APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Examiner:

Appellant's Appeal Brief and the Notice of Appeal included herewith are submitted in response to a Final Rejection mailed 10 March 2009 and the Notice of Non-Compliant Appeal Brief mailed September 8, 2009. Appellant appeals the rejection of pending claims 1, 3-8, 10-22, and 24-30.

This Brief is being filed under the provisions of 37 C.F.R. § 41.37. The filing fee set forth in 37 C.F.R. § 41.20(b)(2) of $1000.00 is submitted herewith. The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or to credit any overpayment, to Deposit Account No. 090449.

1. REAL PARTY IN INTEREST

The real party in interest is the assignee, International Business Machines Corporation, Armonk, New York.

2. RELATED APPEALS AND INTERFERENCES

There are no related appeals, interferences, or judicial proceedings.

3. STATUS OF CLAIMS

The Office Action mailed on 10 March 2009 rejected of claims 1, 10, 13, 17, 24, and 28 under 35 U.S.C. 112 for failing to comply with the written description requirement and maintained the rejection of claims 1, 3-7, 10, 11, 13-21, and 24-30 under 35 U.S.C. 103(a) as being anticipated over Moiroux et al. (US patent No. 7,231,547) in view of Tallam (US Patent No. 6,948,099) and further in view of Strange et al. (US Patent No. 6,965,989). Claims 8, 12, and 22 were rejected under 35 U.S.C. 103(a) as being unpatentable over Moiroux, Tallam, and Strange and further in view of Neuman et al. (US PBPUB No. 20030217299). Claims 2, 9, and 23 have been cancelled. Appellants appeal the rejection of all the claims but will focus arguments on independent claims 1, 10, 13, 17, 24, and 28.

4. STATUS OF AMENDMENTS

Appellants submitted an amendment to the claims on 26 August 2008. Identical claims were submitted with the office action response of 03 February 2009 and entered by the examiner on 18 February 2009.

5. SUMMARY OF CLAIMED SUBJECT MATTER

The claimed subject matter deals with a specific apparatus, system, method, and computer readable medium to rapidly and deterministically save data within volatile memory to a data storage device in response to an abnormal operating condition that threatens a loss of data in the volatile

memory. See the abstract of Appellant's Published Application No. US 2005/0086461 (hereinafter "Specification").

The following quotation of independent claims 1, 10, 13, 17, 24, and 28 include reference numerals and parenthetical references to representative examples of the elements and components recited in each claim in compliance with 37 CFR 41.37(c)(1)(v).

1. An apparatus for rapidly, deterministically transferring data, the apparatus comprising:

a processor (310) configured to process data; [*see, for example, paragraph 44*]

a volatile memory (320) configured to store the data; [*see, for example, paragraph 44*]

a boot control module (330) configured to boot the processor with a standard operating kernel (520) under a normal operating condition and to reboot the processor with a data transfer kernel (620) under an abnormal operating condition that threatens a loss of data in the volatile memory, wherein the reboot occurs without a loss of data within the volatile memory; and [*see, for example, paragraphs 45-48, 49-51, and 55-56*]

the data transfer kernel (620) configured to support a data save operation configured to save data in the volatile memory to a storage device. [*see, for example, paragraphs 46-47 and 55-56*]

10. An apparatus for rapidly, deterministically transferring data to a storage device, the apparatus comprising:

a storage device (350) configured to store data; [*see, for example, paragraph 47*]

a data transfer kernel (620) configured to support data saving operations; and [*see, for example, paragraphs 46-47 and 55-56*]

a computer (upper box of Figure 3) in communication with the storage device, the computer configured to load the data transfer kernel during a reboot procedure in response to an abnormal operating condition that threatens the loss of data in a volatile memory, wherein the reboot occurs without a loss of data within the volatile memory; the data transfer kernel

configured to support a data save operation configured to save data in the volatile memory to the storage device. [*see, for example, paragraphs 45-48, 49-51, and 55-56*]

13. An apparatus for rapidly, deterministically saving data, the apparatus comprising:

means for saving data (340) in a non-volatile memory; [*see, for example, paragraph 46*]

means for detecting a data save condition (410) comprising an abnormal operating condition that threatens the loss of data in a volatile memory; and [*see, for example, paragraph 50*]

means for booting a processor (330) with a data transfer kernel without a loss of data within the volatile memory in response to the abnormal operating condition, the data transfer kernel configured to save data to the means for saving data. [*see, for example, paragraphs 45-48, 49-51, and 55-56*]

17. A system for rapidly, deterministically saving data to a storage device, the system comprising:

a processor (310) configured to process data; [*see, for example, paragraph 44*]

a memory (320) configured to provide volatile storage for the data; [*see, for example, paragraph 44*]

a storage device (350) configured to provide non-volatile storage for the data; [*see, for example, paragraph 47*]

a boot control module (330) configured to boot the processor module with a standard operating kernel under a normal operating condition and to reboot the processor with a data transfer kernel under an abnormal operating condition that threatens the loss of data in the memory, wherein the reboot occurs without a loss of data in the memory; and

the data transfer kernel configured to support a data save operation configured to save data in the memory to the storage device. [*see, for example, paragraphs 45-48, 49-51, and 55-56*]

24. A method for rapidly, deterministically saving data, the method comprising:

detecting a data save condition (Figure 2 step 120) that threatens the loss of data in a volatile memory; and [*see, for example, paragraph 38*]

rebooting a processor module (Figure 2 step 210) with a data transfer kernel (620) configured to support a data save operation configured to save the data in the volatile memory to a non-volatile storage device, wherein rebooting the processor module occurs without a loss of data in the volatile memory. [*see, for example, paragraphs 39, 45-48, 49-51, and 55-56*]

28. A computer readable storage medium comprising computer readable program code for rapidly, deterministically saving data, the program code configured to:

boot a processor module (Figure 2 step 210) with a data transfer kernel (620) configured to support a data save operation (Figure 2 step 240) and in response to an abnormal operating condition that threatens the loss of data in a volatile memory module comprising volatile memory; and [*see, for example, paragraphs 38 and 39*]

transfer the data with the data save operation from the ~~a~~ memory module (320) to a non-volatile storage device, without a loss of data in the memory module (350). [*see, for example, paragraphs 39, 45-48, 49-51, and 55-56*]

The present invention in the various embodiments presented in the foregoing claims, enables the rapid and deterministic saving of data from a volatile memory to a (non-volatile) storage device in response to detecting an abnormal operating condition that threatens a loss of data in the volatile memory. The rapid and deterministic saving of data is accomplished by rebooting a processor with a data transfer kernel that supports data save operations. Rebooting clears the processor of executing processes and frees the processor to execute the data save operation(s) supported by the data transfer kernel. A data transfer kernel is distinguished from a standard operating kernel used in normal operation in that a data transfer kernel supports a limited and dedicated set of software and hardware processes that are required to save data such as configuring a processor and storage devices for data save (*i.e.* data transfer) operations and loading and executing a data transfer process to conduct the data save operations [see paragraphs 39, 55, and 56].

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. Whether the Examiner has properly rejected claims 1, 10, 13, 17, 24, and 28 under 35 U.S.C. 112 for failing to comply with the written description requirement.

II. Whether the Examiner has properly rejected evidence that the Moiroux et al. reference is not prior art.

III. Whether the Examiner has established a *prima facie* case of claims 1, 3-7, 10, 11, 13-21, and 24-30 under 35 U.S.C. 103(a) as being anticipated over Moiroux et al. in view of Tallam (US Patent No. 6,948,099) and further in view of Strange et al. (US Patent No. 6,965,989).

7. ARGUMENT

I. The Examiner has improperly rejected claims 1, 10, 13, 17, 24, and 28 under 35 U.S.C. 112 for failing to comply with the written description requirement.

Appellants should mention, that due to their concerns regarding the Examiners assertion of an inoperable invention and failure to respond to the written description requirement, Appellants representative spoke with the Group Director of Art Unit 2100 concerning the practice at the USPTO regarding inoperable embodiments as a postlude to a conversation involving another matter in different application pending in the office. Based on the characterization provided by the Group Director (*i.e.* a presumption of operability), Appellants representative contacted the Office of the Commissioner where the matter was routed to the Office of Patent Quality Assurance. After review of the particulars of this case, the Office of Patent Quality Assurance confirmed the policy of a presumption of operability and recommended that the rejection under 35 U.S.C. 112 of the present application be vacated. The Board may contact Anthony Caputa of the Office of Patent Quality Assurance at 517-272-0829 for additional details. Furthermore, an interview summary included with the latest office action indicated that the 112 rejection for enablement will be withdrawn. However, since the office action did not officially withdraw the rejection and raised additional issues with regard to a 112 rejection, Appellants have elected to respond to the 112 rejection included in the latest office action.

Appellants submit that claim 1 is representative of the subject matter recited in independent claims 10, 13, 17, 24 and 28. Therefore, Appellants' response will focus on claim 1 with the understanding that responses for claims 10, 13, 17, 24, and 28 would follow a similar vein.

Claim 1 recites:

1. (Previously Amended) An apparatus for rapidly, deterministically transferring data, the apparatus comprising:

a processor configured to process data;

a volatile memory configured to store the data; and

a boot control module configured to boot the processor with a standard operating kernel under a normal operating condition and to reboot the processor with a data transfer kernel under an abnormal operating condition that threatens a loss of data in the volatile memory, wherein the reboot occurs without a loss of data within the volatile memory;

the data transfer kernel configured to support a data save operation configured to save data in the volatile memory to a storage device.

The Examiner asserts that the "*claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention*" and that there is no disclosure for the amended claim limitation: "*wherein the reboot occurs without a loss of data within the volatile memory*". The Examiner then states that appropriate correction is required.

Appellants disagree and assert that the Examiner is disregarding the plain meaning and intent of the Application. Appellants are also somewhat puzzled that the Examiner is asking for correction if the Application fails to "*reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention*".

Appellants assert that it is clear that the intent of the invention is rapidly and deterministically saving data within volatile memory. Furthermore, Appellants assert that it would make no sense to save corrupted data and that the Application is more than sufficiently clear to one of skill in the art that the inventors had possession of the claimed invention at the time the application was filed. For example, the background section of the application states: "*Short-term back-up power supplies are designed to supply power until a computer can safely be shut down. Data residing in the computer's volatile memory* ***must be transferred to non-volatile memory before short-term power is exhausted***." Thus the background section of the patent application clearly indicates the need for

saving data within volatile memory before it is corrupted and a loss of data occurs. This need is confirmed by the last paragraph of the background section which indicates:

> *"What is needed is a device, system, and method of configuring a computer to* ***save data as rapidly as possible*** *during a computer system shutdown. What is more particularly needed is a device, system, and method of deterministically terminating existing processing and configuring a computer and related subsystems to save data from volatile storage to non-volatile storage."*

In addition to communicating the need for saving data before a loss of data occurs in the background section, the specification communicates in a manner that is clear to one of skill in the art that *"the reboot occurs without a loss of data within the volatile memory"*. For example, the summary of the invention states "*Various elements of the present invention are combined into a system* ***for rapidly and deterministically saving data***." Appellants assert that declaring that the invention rapidly and deterministically saves data is a clear indication that the data within the volatile memory is preserved at least until the saving process is completed. Appellants also assert that, even the title of the Application "APPARATUS SYSTEM AND METHOD FOR DETERMINISTICALLY TRANSFERING DATA BY REBOOTING TO A DATA TRANSFER KERNEL" suggests to one of skill in the art that present invention conducts a reboot operation before a loss of data occurs and without corrupting that data.

Appellants are concerned that the Examiner is insufficiently skilled in the art to be able to visualize how the invention is able to transfer data before a loss of data occurs. Appellants assert that the Application is more than sufficiently clear on this issue to one of skill in the art. Appellants note that it is well known to those of skill in that art that virtually all known computer power supplies and memory devices have internal capacitance which prevents immediate loss of data. Furthermore, standard engineering practice requires the inclusion of bypass capacitors on circuit

boards in order to suppress the presence of noise in the power source. The inclusion of bypass capacitors further delays a loss of data after AC power is discontinued to the DC power supply of a computer. Also, standard practice for enterprise computing systems provides for a backup power supply or the like (often a battery-based inverter) that may provide temporary short-term power (as mentioned in the background section) when a power failure occurs.

Appellants note that a detection of a loss in power is typically accomplished by monitoring AC power previous to filtering, conditioning, and conversion to DC. Therefore, it is well know to those of skill in the art that a loss of (input) power occurs well before a loss of data occurs within standard computing systems particularly in installations that are designed to reduce data loss. Appellants submit that communication of these well known and understood characteristics and practices is not required to show possession of the invention but may be a source of confusion to those that are not skilled in the art.

Despite the well known delay between a loss of power and an actual loss of data, computing systems have typically been unable to reliably save data as communicated by the background section of the application as follows:

> *"In such conditions, processes are susceptible to completion delays and faults that may result in failure to return control to the operating kernel. Furthermore, as processes delay or stall, computer operation may become increasingly unstable and the computer's standard operating kernel may ultimately stall, losing valuable data, even though the computer was continuously powered with back-up power."*
>
> *"A data saving process that saves data during a power failure or other shutdown operation typically runs under the computer's standard operating kernel. The data saving process may be slowed by existing processes that were already running under the standard operating kernel before the power failure occurred. The existing processes may stall before the data transfer can be completed. Existing*

processes also take processing power and communications bandwidth from the critical data saving process, and can potentially cause unacceptable non-deterministic delays during the data transfer process. Even shutting down the existing processes can be unpredictable if power failure conditions prevent normal process termination. The delays of existing processes put the computer's ability to rapidly and predictably save data during a power failure shutdown at risk."

The specification and claims disclose a concise solution to the problem of stalled processes and unreliable shutdowns during power failures that is presented in the background section of the application. For example, the summary of the invention states:

"In one embodiment, a boot control module detects a condition such as a power failure requiring a rapid, deterministic data save procedure. To initiate the data save operation, the boot control module reboots the processor. All previously existing processes including the standard operating kernel are deterministically terminated by the reboot."

Appellants submit that it is extremely clear to one of skill in the art that rebooting prevents existing processes from stalling a computer system and can therefore occur *"without a loss of data within the volatile memory"* due to the inherent delay between a loss of power and a loss of data. Appellants therefore assert that originally submitted specification is clear and definite that the "*reboot occurs without a loss of data within the volatile memory*" as submitted in the amendment of 26 August 2008.

Appellants also submit it is improper to assume that the reboot occurs with a loss of data. To assume that a loss of data occurs, would require the reader to assume that the claimed invention is inoperable despite the solutions presented in the specification to provide *"a rapid, deterministic data save operation"* and despite the knowledge of those of skill in the art that a detection of a loss of power condition can occur well before a loss of data occurs within a computing system. Appellants

also submit than any invention that can reduce the time it takes to save data has utility and is entitled to a patent even if some implementations of the invention do not work under every circumstance – particularly if the results are superior under most circumstances.

Appellants note that during prosecution the Examiner has spent considerable time focusing on the definition of the term "reboot" and how some implementations of reboot could render the invention inoperable. In particular, the Examiner asserts that a cold reboot or a reboot that clears memory would be inoperable. Appellants concede that some adjustments may be required (or preferred) in order to ensure that the reboot does not render the invention operable. Appellants assert however that such adjustments are within the working knowledge of those of skill in the art and do not fit within the realm of undue experimentation.

With regard to this issue Appellants take exception to how the Examiner has presented the evidence regarding whether a reboot is a cold reboot that shuts down power to the memory and processor or a warm reboot that continues to provide power to the processor and memory. A careful review will show that both scenarios are supported substantially equally within the lexicons cited by the Examiner. However, the Examiner has presented the evidence in a misleading manner that suggests that a warm reboot is not supported as much as a cold reboot in the cited lexicons.

Furthermore, Appellants assert that it is understood by those of skill in the art that reboot procedures initiated under software and/or electronic control as required by the claim limitation "*a boot control module configured to boot the processor with a standard operating kernel under a normal operating condition and to reboot the processor with a data transfer kernel under an abnormal operating condition*" are almost always warm reboot procedures that do not interrupt power to the processor and memory. Thus an operable reboot such as a warm reboot is inferred by the claims particularly when interpreted in light of the specification. Furthermore, one of skill in the art would not be motivated to interpret the claims in a manner which renders the claimed invention inoperable.

The Examiner also asserts that if the reboot procedure is a hard/cold reboot that the volatile memory would be erased. Although a warm reboot is inferred by the claims and obviously preferred, Appellants assert that the Examiner's assumption that a cold/hard reboot is inoperable is not necessarily true. As indicated above, removal of input power does not result in immediate loss of data.

Early users of personal computers were very familiar with the need to turn off a computer to for at least several seconds to clear the working memory of the computer in response to a system crash or a virus. For example, early versions of the IBM personal computer required that the computer be put in the off condition for at least several seconds to effectively clear the memory due to the capacitance of the memory cells and the DC power supply. Even today, Symantec corporation has the following instructions on their web site (see http://www.symantec.com/security_response/writeup.jsp?docid=2003-081915-0030-99) when dealing with a certain virus:

> Note: If, when running the tool, you see a message that the tool was not able to remove one or more files, run the tool in Safe mode. Shut down the computer, turn off the power, and wait 30 seconds. Restart the computer in Safe mode and run the tool again.

Note the necessity of turning off the computer for an extended length of time to ensure that the working (*i.e.* volatile) memory is cleared and the virus is no longer present within the program memory of the computer. Appellants assert that this is sufficient evidence that a quickly executed cold reboot would not erase the memory unless the memory was intentionally erased by a shutdown routine. Furthermore, since the objective of the invention is to save data as quickly and deterministically as possible, one must assume a quickly executed reboot without intentional erasure. Therefore the data would likely remain valid even with a hard/cold reboot. Appellants therefore assert that the assumption that a cold boot procedure would be inoperable is conjecture.

Appellants also note the following description of a cold boot attack from http://en.wikipedia.org/wiki/Cold_boot_attack. A cold boot attack "*relies on the data remanence property of DRAM[2] and SRAM[3] to retrieve memory contents which remain readable in the seconds to minutes after power has been removed.*" Appellants submit that knowledge of the data remanence property of DRAM and SRAM is common to those of skill in the art and is conclusive evidence that it is improper to assume that rebooting with a cold boot procedure would render the claimed invention inoperable. Therefore it would be improper to restrict the claimed invention to a cold boot or a warm boot embodiment.

Appellants acknowledge that rebooting with a cold boot procedure is probably not preferred but also admit that it may be preferred in certain unique circumstances. Appellants assert that selection of a cold boot or a warm boot procedure and the details associated therewith is within the working knowledge of one of skill in the art and that the specification need not disclose such details to be enabling.

Appellants question whether it is necessary (or legal to require) that the language of a claim explicitly exclude possibly inoperable interpretations or embodiments. Appellants submit that virtually any invention could be embodied in an inoperable form and still fit within the scope of the claims of an issued patent. Appellants rhetorically ask if it would be proper to invalidate each issued patent that includes a possible inoperable embodiment within the scope of the claims of the issued patent. Appellants note that there is no need to protect the public from inoperable embodiments by denying an Applicant intellectual property that includes inoperable embodiments since inoperable embodiments are of no value to society and no consequence in the marketplace.

Appellants assert that inventors are entitled to a presumption of operability with regard to how one of skill in the art would implement an invention. Appellants also assert that it is inappropriate to assume that the claimed invention is inoperable particularly when one of skill in the art would appreciate the effectiveness of rebooting to "*a data transfer kernel configured to support a*

data save operation configured to save data in the volatile memory to a storage device." Given the clarity of the specification on providing rapid and deterministic means and methods for saving data within a volatile memory to a non-volatile storage device, Appellants assert that there is clear and sufficient evidence that "*that the inventors, at the time the application was filed, had possession of the claimed invention*" as well as support for the claimed limitation of "*wherein the reboot occurs without a loss of data within the volatile memory*". Therefore, the rejection under 35 U.S.C. 112 is improper.

II. The Examiner has improperly rejected evidence that Moiroux et al. is not prior art.

Exhibits A-D were submitted by Appellants on 2/3/2009. Exhibit B was initially presented internally within IBM corporation on 6/26/2002 (as indicated on the title page) and last updated on 8/6/2002 as indicated by the timestamp on the electronic file. Page 18 of Exhibit B indicates that the "firehose dump of NVS memory" which is to be triggered by a 'battery at threshold' message is a planned feature of the ESS firmware. Subsequently, the IBM disclosure document marked Exhibit A indicates that the 'main idea of the invention' which is described therein as a 'firehose dump' was submitted on 10/22/2002. Appellants assert that the submitted IBM disclosure document marked Exhibit A shows possession of the invention by the inventors on or before 10/22/2002. The IBM disclosure document was subsequently evaluated, commented on, and rated on 11/13/2002, with a final decision on preparing a patent application made on 04/16/2003 with a planned filing date of 7/18/2003. Exhibit C indicates that a letter was sent from IBM Attorney Dale M. Crockatt to Attorney Brian Kunzler of Kunzler and Associates on 4/16/2003 requesting preparation of a patent application. Exhibit D indicates that an initial draft of the patent application was sent to inventor Yu-Cheng (Vincent) Hsu on or after 7/10/2003.

Following the standard procedure of Kunzler and Associates at the time, the initial draft was subsequently reviewed by inventor Yu-Cheng (Vincent) Hsu at his earliest convenience, updated by Scott Thorpe, reviewed by Attorney Brian Kunzler for quality, and sent to all of the inventors for final review and signing. Additional drafts may also have been processed. According to the Oath

and Declaration stored in the image file wrapper of the USPTO, the inventors signed the Oath and Declaration on 10/13/2003 and 10/14/2003. The application was subsequently filed on 10/16/2003.

Appellants submit that the evidence shows that the claimed invention was conceived on or before 10/22/2002, which is previous to the U.S. filing date of Moiroux of 3/29/2003 and the publication date of Moiroux of 12/11/2003, and was followed by diligence in reducing the invention to constructive practice. Rule 131 Affadavits from attorney Brian Kunzler and inventor Yu-Cheng (Vincent) Hsu attesting to the truthfulness of the preceding evidence were submitted to the USPTO along with the evidence on 2/3/2009.

III. The Examiner has not established a *prima facie* case of claims 1, 3-7, 10, 11, 13-21, and 24-30 under 35 U.S.C. 103(a) as being anticipated over Moiroux et al. in view of Tallam (US Patent No. 6,948,099) and further in view of Strange et al. (US Patent No. 6,965,989).

A review of the present invention may help clarify the novelty of Appellants' claims over the cited prior art. Referring to the written descriptions of Figures 1 and 2 of the application, a processor is booted with a standard operating kernel that supports normal operating conditions. Under normal operating conditions, data is stored in a volatile memory. If an abnormal operating condition that threatens the loss of data in the volatile memory is detected, the processor is rebooted with a data transfer kernel. Rebooting frees the processor of any previously running processes that may prevent deterministic execution and thereby enables the processor to run a data save operation supported by the data transfer kernel in a rapid deterministic manner. The data save operation saves the data located in the volatile memory to a non-volatile storage device.

Appellants arguments will focus on the elements of independent claim 1 with the understanding that the same arguments also apply to the elements delineated in independent claims 10, 13, 17, 24, and 28.

The Examiner acknowledges that "*Moiroux does not specifically disclose rebooting with a different kernel under an abnormal operating condition that threatens a loss of data*" but asserts that Tallam col. 5 lines 5-10; col. 3 lines 48-49; col. 4 lines 13-17; col. 3 lines 33-36 discloses "*reboot[ing] the processor under an abnormal operating condition that threatens a loss of data*".

Applicants strongly disagree with the Examiners assertion for at least the following at least the following reasons:

- The reboot of Tallim is not in response to *"an abnormal operating condition that threatens a loss of data"*. Neither Tallim nor Moiroux disclose such a reboot.
- Contrary to the characterization of the Examiner, the claimed invention is for a "data transfer kernel" and not a "different kernel". However, neither Tallim nor Moiroux discloses a *"data transfer kernel"*.

A review of Tallim may clarify the differences between the prior art and the claimed invention. Tallim discloses methods for recovering a primary operating system that has been corrupted or is out of date. As shown in Figure 4 and described in Column 4 lines 29-34 Tallim teaches:

> *"Upon power up, after going through the power on self test (POST), the start-up code checks the primary operating system image in the memory 14 for checksum errors. If there is an error, the system boots the recovery operating system 20 and launches the recovery application."*

Figure 3 also clearly shows that Tallim uses an 'OS RECOVERY AND UPDATE APPLICATION' 24 (that is not part of the kernel) to recover or update the primary operating system. Therefore, the reboot of Tallim is not in response to *"an abnormal operating condition that threatens a loss of data"*. Furthermore, the kernel of Tallim is not directed to specialized operations such as data saving operations as suggested by the Examiner.

The use of a "data transfer kernel" is an important aspect of the claimed invention that is not disclosed in Tallim nor Moiroux. Consider the following definition of Kernel from Webopedia:

> Kernel
>
> The central module of an operating system. It is the part of the operating system that loads first, and it remains in main memory. Because it stays in memory, it is important for the kernel to be as small as possible while still providing all the essential services required by other parts of the operating system and applications.

While Moiroux does disclose a data backup utility or application and Tallim an 'OS RECOVERY AND UPDATE APPLICATION', Appellants assert that neither Moiroux nor Tallim discloses "a data transfer kernel configured to support a data save operation". The use of a kernel dedicated to data save operations provides additional functionality over a data backup utility or application including immediate accessibility, a deterministic execution time, and faster execution since the computer does not need to continually switch context between the operating system kernel and an application or utility. For example, a typical computer must switch state between the supervisor privileges associated with ring 0 (*i.e.* kernel) processes and the user privileges of outer ring processes that are executed by applications and utilities. The overhead for such context switching can considerably reduce performance and make the computing system more vulnerable to malware such as viruses.

Appellants therefore assert that the cited prior art does not suggest or teach a motivation for providing a data transfer kernel configured to support a data save operation and rebooting to that kernel.

In contrast to Moiroux and Tallim, Appellants disclose a solution for saving data in volatile memory to a non-volatile memory in response to abnormal operating conditions by rebooting to a data transfer kernel. As such, Appellants respectfully assert that the prior art and the present invention cover processes that are not only distinct in terms of claim elements, but are distinct in perspective and objectives as well.

In addition to not disclosing a data transfer kernel, Appellants submit that Moiroux and Tallim do not disclose "a boot control module configured to ... reboot the processor with a data transfer kernel under an abnormal operating condition that threatens a loss of data in the volatile memory". Appellants submit that the rebooting that occurs in Tallim is a post-mortem boot that occurs well after a failure and not "under an abnormal operating condition that threatens a loss of data in the volatile memory".

Given the foregoing, Appellants respectfully assert that Moiroux and Tallim fail to anticipate the present invention. More particularly, Moiroux and Tallim fail to disclose, suggest, teach, or provide a motivation for rapidly and deterministically transferring data by *"reboot[ing] a processor with a data transfer kernel under an abnormal operating condition that threatens a loss of data in*

volatile memory".

SUMMARY

In view of the foregoing, Appellants respectfully assert that each of the claims on appeal have been improperly rejected because the Examiner has failed to show that Moiroux in combination with Tallim anticipates each of the limitations of independent claims 1, 10, 13, 17, 24, and 28. Furthermore, Appellants assert that the Examiners assertion that the specification was not enabling was misplaced and unfounded and valid evidence that Moiroux was not prior art was ignored.

Respectfully submitted,

Date: October 8, 2009

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8. CLAIMS APPENDIX

Claims involved in the appeal

1. (Previously Amended) An apparatus for rapidly, deterministically transferring data, the apparatus comprising:

a processor configured to process data;

a volatile memory configured to store the data;

a boot control module configured to boot the processor with a standard operating kernel under a normal operating condition and to reboot the processor with a data transfer kernel under an abnormal operating condition that threatens a loss of data in the volatile memory, wherein the reboot occurs without a loss of data within the volatile memory; and

the data transfer kernel configured to support a data save operation configured to save data in the volatile memory to a storage device.

2. (Canceled)

3. (Previously Amended) The apparatus of claim 1, wherein the data save operation is selected from the group consisting of a storage configuration operation, a transfer process loading operation, a data transfer operation, and a system shutdown operation.

4. (Original) The apparatus of claim 3, wherein the data transfer kernel is configured to exclusively support the data save operation.

5. (Previously Amended) The apparatus of claim 1, further comprising a memory module comprising data bits for marking data to be saved during the data save operation.

6. (Original) The apparatus of claim 5, wherein the standard operating kernel is further configured to mark data to be saved during a data save operation.

7. (Original) The apparatus of claim 1, wherein the data transfer kernel is configured to configure the storage device for specialized data save operations.

8. (Original) The apparatus of claim 1, wherein the data transfer kernel is configured to conduct a power down procedure.

9. (Canceled)

10. (Previously Amended) An apparatus for rapidly, deterministically transferring data to a storage device, the apparatus comprising:

a storage device configured to store data;

a data transfer kernel configured to support data saving operations; ~~and~~

a computer in communication with the storage device, the computer configured to load the data transfer kernel during a reboot procedure in response to an abnormal operating condition that threatens the loss of data in a volatile memory, wherein the reboot procedure occurs without a loss of data in the volatile memory; and

the data transfer kernel configured to support a data save operation configured to save data in the volatile memory to the storage device.

11. (Original) The apparatus of claim 10, wherein the data transfer kernel is configured to exclusively support devices and processes required to save data to the storage device.

12. (Original) The apparatus of claim 10, wherein the data transfer kernel is configured to power down the computer and the storage device.

13. (Previously Amended) An apparatus for rapidly, deterministically saving data, the apparatus comprising:

means for saving data in a non-volatile memory;

means for detecting a data save condition comprising an abnormal operating condition that threatens the loss of data in a volatile memory; and

means for booting a processor with a data transfer kernel without a loss of data in the volatile memory in response to the abnormal operating condition, the data transfer kernel configured to save data to the means for saving data.

14. (Original) The apparatus of claim 13, further comprising means for configuring the means for saving data for data save operations.

15. (Original) The apparatus of claim 13, further comprising means for booting a standard operating kernel for normal operation.

16. (Original) The apparatus of claim 13, further comprising means for marking data to be saved during a data save operation.

17. (Previously Amended) A system for rapidly, deterministically saving data to a storage device, the system comprising:

a processor configured to process data;

a memory configured to provide volatile storage for the data;

a storage device configured to provide non-volatile storage for the data; ~~and~~

a boot control module configured to boot the processor module with a standard operating kernel under a normal operating condition and to reboot the processor with a data transfer kernel under an abnormal operating condition that threatens the loss of data in the memory, wherein the reboot occurs without a loss of data in the memory; and

the data transfer kernel configured to support a data save operation configured to save data in the memory to the storage device.

18. (Previously Amended) The system of claim 17, wherein the standard operating kernel is configured to mark data in the memory to be saved by the data transfer kernel during a data save operation.

19. (Previously Amended) The system of claim 17, wherein the data transfer kernel exclusively supports devices, operations, and processes required to save data.

20. (Original) The system of claim 17, wherein the data transfer kernel configures the processor for data saving operations.

21. (Original) The system of claim 17, wherein the data transfer kernel configures the storage device for specialized data saving operations,

22. (Original) The system of claim 17, wherein the data transfer kernel is configured to conduct a power down procedure.

23. (Canceled)

24. (Previously Amended) A method for rapidly, deterministically saving data, the method comprising:

detecting a data save condition that threatens the loss of data in a volatile memory; and

rebooting a processor module with a data transfer kernel configured to support a data save operation configured to save the data in the volatile memory to a non-volatile storage device, wherein rebooting the processor module occurs without a loss of data in the volatile memory.

25. (Previously Amended) The method of claim 24, further comprising exclusively supporting devices, operations, and conducting processes required to save data to a storage device.

26. (Previously Amended) The method of claim 24, further comprising configuring the non-volatile storage device to receive data.

27. (Original) The method of claim 24, further comprising marking data to be saved by the data transfer kernel.

28. (Previously Amended) A computer readable storage medium comprising computer readable program code for rapidly, deterministically saving data, the program code configured to:

boot a processor module with a data transfer kernel configured to support a data save operation and in response to an abnormal operating condition that threatens the loss of data in a volatile memory module comprising volatile memory; and

transfer the data with the data save opeartion from the ~~a~~ memory module to a non-volatile storage device without a loss of data in the memory module.

29. (Original) The computer readable storage medium of claim 28, wherein the computer readable code is further configured to mark data in the memory module to be saved to the storage device.

30. (Previously Amended) The computer readable storage medium of claim 28, wherein the computer readable code is further configured to exclusively support devices, operations, and processes required to save data to the storage device.

9. EVIDENCE APPENDIX

The following were submitted to the USPTO as non-patent literature on 2/3/2009:

Exhibit A (TUC920030050US1_ExhibitA.pdf) – IBM Disclosure Document TUC8-2002-0172 created on 10/22/2002 and last modified on 4/16/2002.

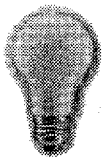
Exhibit B (TUC920030050US1_ExhibitB.pdf) – IBM Enterprise Storage Server Megamouth Authored by Inventor Rick Ripberger and presented on 6/26/2002 and last saved on 8/6/2002.

Exhibit C (TUC920030050US1_ExhibitC.pdf) – Letter to Attorney Brian Kunzler from IBM dated 4/16/2003

Exhibit D (TUC920030050US1_ExhibitD.pdf) – Email correspondence dated 7/10/2003 between patent practitioners Scott Thorpe and Steve McDaniel of Kunzler and Associates concerning sending the initial draft of patent application to Inventor Yu-Cheng (Vincent) Hsu.

Appellants have included selected excerpts from Exhibits A and B herein for the convenience of the review board. Exhibits C and D are included in their entirety:

Exhibit A



Disclosure TUC8-2002-0172

Prepared for and/or by an IBM Attorney - IBM Confidential

Created By Vincent Hsu On 10/22/2002 01:30:15 PM MDT
Last Modified By Roi-Ann Mullis On 04/16/2003 02:57:39 PM MDT

Required fields are marked with the asterisk (*) and must be filled in to complete the form .

***Title of disclosure (in English)**

High Reliability Power Loss Recovery

Summary

Status		Final Decision **(File)**
Final Deadline		07/18/2003
Final Deadline Reason		
Docket Family		TUC9-2003-0050
*Processing Location		Tucson
*Functional Area	select	(Vogel) Storage Controller Microcode
Attorney/Patent Professional		Dale M Crockatt/Burlington/IBM
IDT Team	select	Michael Hartung/Tucson/IBM Nancy Skawski/Tucson/Contr/IBM Bob Bartfai/Tucson/IBM
Submitted Date		10/22/2002 01:46:48 PM MDT
*Owning Division	select	SPD
Incentive Program		
Lab		
*Technology Code		371
PVT Score		

Inventors with a Blue Pages entry

Inventors: Vincent Hsu/Tucson/IBM, Richard Ripberger/Tucson/IBM

Inventor Name	Inventor Serial	Div/Dept	Inventor Phone	Manager Name
> Hsu, Yu-Cheng (Vincent)	652347	2D/2QLA	321-4298	Kolvick, Robert J. (Bob)
Ripberger, Richard A.	853892	2D/DLWA	321-2269	Puldy, Michael L.

> denotes primary contact

***Main Idea**

1. Background: What is the problem solved by your invention? Describe known solutions to this problem (if any). What are the drawbacks of such known solutions, or why is an additional solution required? Cite any relevant technical documents or references.

Firehose dump is to dump customer's data to a groups of dedicated disks in the event of losing utility power. An unsucessfully firehose dump will result in losing customer data. It is important to guarantee the success of the firehose dump process.

In the event of power loss, there are lots of processes running in the operating environment. If some process contaminats the operating system or data structure, Firehose dump may fail.

2. Summary of Invention: Briefly describe the core idea of your invention (saving the details for questions #3 below). Describe the advantage(s) of using your invention instead of the known solutions described above.

This invention is to execute firehose dump by reboot the system again. This will terminate most of the processes and put firehose dump executable in a "saver" environment. Therefore the reliability of firehose dump is greatly improved.

3. Description: Describe how your invention works, and how it could be implemented, using text, diagrams and flow charts as appropriate.

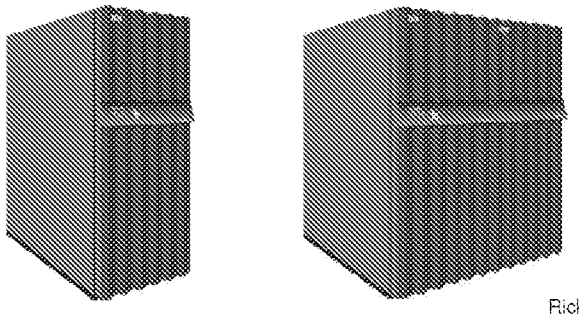
To improve the success of the firehose dump, in the event of power loss, the system will reboot first with the EPOW recovery flag. The EPOW recovery reboot will configure the FHD disks first and then boot up the firehose dump kernel. Since the Firehose dump occurs during the reboot environment, the number of process running in the system is very few and under controllered. Therefore the Firehose dump reliability is greatly improved.

The second part of this invention is to in the reboot process. The firehose dump process will be initantiated right after the firehose dump disks are configured. Once firehose dump process is completed, the system power will be shutdowned. Not full operation system will be broght up.

Exhibit B
Page 1:

Enterprise Storage Server

Megamouth / PHYP Overview



Rick Ripberger
IBM Tucson
June 26, 2002

Page 18:

ESS Firmware Requirements

- Partner LPARs
  - LPARs in Two CECs (Multi-Hub)
  - Adapter Sharing
    - Adapters in Both AIX Device Trees
    - Shared Access from Both LPARs via Memory Sharing
  - Memory Sharing
    - Messaging and DMA between LPARs
    - Messaging and DMA Between LPAR and Adapter
    - One LPAR sets up TCEs to Both CEC Memories
  - Product Type/Model and Partner Identification In Profile
- ~~Memory Allocations Distributed Across Memory Controllers~~
- Memory Preserving IML/IPL of NVS/Cache Regions
- Firehose Dump of NVS Memory
  - Open Firmware - Must Run Independently of AIX / ESS Code
  - Dumps NVS Memory to Local Disk When Enabled by ESS Code
  - Triggered by Battery At Threshold Message, Wait N Seconds and Dump

Exhibit C

Intellectual Property Law Department
9000 South Rita Road, Tucson, Arizona 85744
General Phone Number: 520-799-5025, FAX: 520-799-5551
E-mail: crockatt@us.ibm.com

VIA AIRBORNE MAIL

April 16, 2003

Brian C. Kunzler
10 West 100 South
Suite 425
Salt Lake City, Utah 84101

ATTENTION: Brian Kunzler

Subject: U.S. Patent Application for
"HIGH RELIABILITY POWER LOSS RECOVERY"
Inventor: Y. Hsu, et.al.
IBM Docket No.: TUC920030050US1

Dear Brian,

Enclosed please find a copy of the disclosure, prior art search results and inventor information for the above-identified docket. Please proceed with the preparation of a patent application based on the enclosed. Your inventor contact is Vincent Hsu, who can be reached at (520) 799-4298. Please contact the inventor as soon as possible to begin preparation of the application for a filing date not later than July 18, 2003. Please contact me in advance if you anticipate not meeting this deadline.

Please review the enclosed copy of the IBM San Jose / Tucson Outside Counsel Guidelines thoroughly prior to commencing preparation. If work will be assigned to another member or associate of the firm, please assure that she or he has a complete understanding of such Guidelines and the matters discussed in this letter prior to commencing work on this application.

Please prepare a specification describing multiple embodiments, which may require you to have additional discussions with the inventor(s). Also, please prepare broad, moderate, and narrow claim sets which may include up to about 30 claims. If you find that you will be requiring more than 30 claims to properly prepare this application, please contact me to discuss.

The total amount for preparation of this application is authorized at no more than $5,000.00 for the entire set of application documents described in the Outside Counsel Guidelines. Please note this amount includes the preparation and filing of the patent application (exclusive of draftsman and USPTO fees), a Declaration and Power of Attorney (signed by the inventors), Assignment, an Information Disclosure Statement (IDS), and the formal drawings at the time of filing, as more particularly set forth in the Guidelines. If you believe it will cost more to prepare this application, please contact me before commencing preparation of this application. Please do not exceed this total amount without express written authorization from me.

Please let me know if you need anything further. Thank you for your assistance in filing this application.

Sincerely yours,

Dale M. Crockatt/rpm

Dale M. Crockatt
Tucson Intellectual Property Law Counsel

DMC/rpm
Enclosures

Exhibit D

From: THORPE SCOTT [THORPES@law.utah.edu]
Sent: Thursday, July 10, 2003 3:17 PM
To: 'Steve McDaniel '
Subject: RE: 1514

Steve,
No problem. I will send it out a little later this afternoon.
Scott

-----Original Message-----
From: Steve McDaniel
To: THORPE SCOTT
Sent: 7/10/2003 9:30 AM
Subject: RE: 1514
Scott,
I am sending a bar date application(July 15th) to Vicent Hsu this morning. I would prefer that you wait until this afternoon to send yours unless it is going to another inventor.
Regards,
Steve

-----Original Message-----
From: THORPE SCOTT [mailto:THORPES@law.utah.edu]
Sent: Thursday, July 10, 2003 8:54 AM
To: 'stevemcdaniel@utahpatentlaw.com'
Subject: 1514
Steve,
Thank you for the edits. Unless you feel otherwise, I will send this off to the inventor today as the due date is coming up.
Scott

10. RELATED PROCEEDINGS APPENDIX

None.